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10/743,422	12/23/2003	Sebastien Hily	2207/17041	7513

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EXAMINER

PETRANEK, JACOB ANDREW

ART UNIT	PAPER NUMBER
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2183

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/743,422	HILY ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 February 2007.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-6 and 8-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-6 and 8-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-6 and 8-30 are pending.
2. The office acknowledges the following papers:

Claims and arguments filed on 2/16/2007.

New Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-6 are rejected under 35 U.S.C. §103(a) as being unpatentable over Abramson et al. (U.S. 5,751,983), in view of Tran et al. (U.S. 6,065,103).

5. As per claim 1:

Abramson disclosed a processor comprising:

A decoder to decode a load instruction naming a destination register (Abramson: Figure 2 element 201, column 5 lines 12-26)(The load instruction is inherently decoded before it's issued to the execution unit.);

A memory ordering buffer to maintain a store instruction (Abramson: Figure 4 element 503, column 7 lines 62-67 continued to column 8 lines 1-8); and

Abramson failed to teach a trailing store buffer to maintain an address for said store instruction, if said store instruction has been de-allocated from said memory ordering buffer, said trailing store buffer to maintain the address for said source store

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instruction to disambiguate said load instruction.

However, Tran disclosed a trailing store buffer to maintain an address for said store instruction, if said store instruction has been de-allocated from said memory ordering buffer (Tran: Figures 2 and 3 element 44, column 11 lines 1-8)(The speculative store buffer stores non-speculative stores when a store instruction retires. The store instruction is put into the speculative store buffer at the same time that the data is stored in the data cache. Figure 3 shows the buffer storing the address and the data of the store instruction. It's obvious to one of ordinary skill in the art at the time of the invention that upon the store data being transferred to the data cache, the store instruction has retired, which when in combination with Abramson, results in deallocation of a store entry in the memory ordering buffer.), said trailing store buffer to maintain the address for said source store instruction to disambiguate said load instruction (Tran: Figures 2, 3, and 4 elements 44, 64, 86, and 88, column 14 lines 30-65)(Element 64 is the address of the store instruction contained within the speculative store buffer. Element 86 shows that the data within the speculative store buffer is checked against load instructions and element 88 shows that data is forwarded to load instructions.)

The advantage of the speculative store buffer is that it stores the most recent data values for memory addresses, thus only a single hit for a memory address is allowed, which reduces complexity and allows for increased performance (Tran: Column 3 lines 16-35). One of ordinary skill in the art would have been motivated to add the speculative store buffer for the advantage of increased performance. Thus, it would

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have been obvious to one of ordinary skill in the art at the time of the invention to implement a speculative store buffer for the advantage of increased performance for memory operations.

6. As per claim 2:

Abramson and Tran disclosed the processor of claim 1 wherein said memory ordering buffer further comprises:

A store address buffer to maintain the address for said source store instruction (Abramson: Figure 6 element 802, column 8 lines 44-61).

7. As per claim 3:

Abramson and Tran disclosed the processor of claim 1 wherein said memory ordering buffer further comprises:

A store data buffer to maintain data associated with said source store instruction (Abramson: Figure 3 element 304, column 7 lines 18-26)(The Memory Interface Unit that contains the store data buffer is coupled to the Memory Execution Unit that contains the memory ordering buffer. It would have been obvious to one of ordinary skill in the art at the time of the invention that the store data buffer could be placed within the memory-ordering buffer. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

8. As per claim 4:

Abramson and Tran disclosed the processor of claim 1 further comprising:

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A store data buffer coupled to said memory ordering buffer (Abramson: Figure 3 element 304, column 7 lines 18-26)(The Memory Interface Unit that contains the store data buffer is coupled to the Memory Execution Unit that contains the memory ordering buffer.).

9. As per claim 5:

Abramson and Tran disclosed the processor of claim 1 wherein said trailing store buffer is coupled to said memory ordering buffer (Abramson: Figure 5 element 602, column 8 lines 21-32)(The data array is a buffer that temporarily stores data and their corresponding addresses that are originally from a store instruction. Entries received from the MOB are de-allocated at the MOB and are written to the data array. Thus, it reads on a trailing store buffer as claimed. The data array is coupled to the memory ordering buffer.).

10. As per claim 6:

Abramson and Tran disclosed the processor of claim 1 wherein said memory ordering buffer comprises said trailing store buffer (Abramson: Figure 6 element 802, column 8 lines 21-32)(The data array is a buffer that temporarily stores data and their corresponding addresses that are originally from a store instruction. Entries received from the MOB are de-allocated at the MOB and are written to the data array. Thus, it reads on a trailing store buffer as claimed. The data array is coupled to the memory ordering buffer. It would have been obvious to one of ordinary skill in the art at the time of the invention that the memory ordering buffer could be combined with the data array

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into one unit. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

Maintained Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. Claims 8-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Abramson et al. (U.S. 5,751,983), in view of Tran et al. (U.S. 6,065,103).

13. As per claim 8:

Abramson disclosed a method comprising:

Computing a store address (Abramson: Figure 3 element 300, column 7 lines 10-17)(Computing a store address is inherent for a store instruction.);

Writing the store address in a first storage (Abramson: Figure 6 element 802, column 8 lines 44-61)(The store address buffer holds the addresses from store instructions.);

Writing data associated with the store address to a memory (Abramson: Figure 3 element 304, column 7 lines 18-26)(The store data buffer contains the data corresponding to store instructions.);

De-allocating the store address from the first storage (Abramson: Figure 6 element 802, column 8 lines 44-61)(It's obvious to one of ordinary skill in the art that

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entries within the store address buffer are de-allocated when the store instruction retires.);

Predicting a load instruction to be memory renamed (Abramson: Figure 11, column 12 lines 31-47 and column 14 lines 2-18)(Memory renaming can occur when a load instruction is believed to relate to a previous store instruction. A speculative load is done when store instructions do not have addresses that are valid and is believed to relate to one of the load instructions.);

Computing a load store source index (Abramson: Column 12 lines 21-31)(A load store source index can be a store buffer identification (SBID). SBID's are assigned to load instructions.);

Computing a load address (Abramson: Column 9 lines 47-64);

Disambiguating the memory renamed load instruction (Abramson: Figure 11, column 14 lines 19-31)(The speculated load instruction is checked to make sure it obtained the correct data.); and

Retiring the memory renamed load instruction, if the store address is still allocated in at least one of said first storage and said second storage (Abramson: Figure 11, column 14 lines 19-31)(The load instruction is retired if an address matches in the store address buffer.).

Abramson failed to teach allocating the store address in a second storage.

However, Tran disclosed allocating the store address in a second storage (Tran: Figures 2 and 3 element 44, column 11 lines 1-8)(The speculative store buffer stores non-speculative stores when a store instruction retires. The store instruction is put into

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the speculative store buffer at the same time that the data is stored in the data cache.

Figure 3 shows the buffer storing the address and the data of the store instruction.).

The advantage of the speculative store buffer is that it stores the most recent data values for memory addresses, thus only a single hit for a memory address is allowed, which reduces complexity and allows for increased performance (Tran: Column 3 lines 16-35). One of ordinary skill in the art would have been motivated to add the speculative store buffer for the advantage of increased performance. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a speculative store buffer for the advantage of increased performance for memory operations.

14. As per claim 9:

Abramson and Tran disclosed the method of claim 8 wherein computing a store address comprises:

Computing an address for a store instruction (Abramson: Figure 3 element 300, column 7 lines 10-17)(Computing a store address is inherent for a store instruction.).

15. As per claim 10:

Abramson and Tran disclosed the method of claim 8 wherein writing the store address in a first storage comprises:

Writing the store address in a store address buffer (Abramson: Figure 6 element 802, column 8 lines 44-61)(The store address buffer holds the addresses from store instructions. The memory ordering buffer contains the store address buffer.).

16. As per claim 11:

Abramson and Tran disclosed the method of claim 10 wherein writing data associated with the store address to a memory comprises:

Writing the data from said store data buffer to said memory using the store address in said store address buffer (Abramson: Figure 5 element 602, column 8 lines 21-32)(The data array is a buffer that temporarily stores data and their corresponding addresses that are originally from a store instruction. Entries received from the MOB are de-allocated at the MOB and are written to the data array.).

17. As per claim 12:

Abramson and Tran disclosed the method of claim 11 wherein said store data buffer is in the first storage (Abramson: Figure 3 element 304, column 7 lines 18-26)(The Memory Interface Unit that contains the store data buffer is coupled to the Memory Execution Unit that contains the memory ordering buffer. It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the store data buffer in the memory ordering buffer that contains the store address buffer. In addition, according to "In re Japikse" (181 F.2d 1019, 86 USPQ 70 (CCPA 1950)), shifting the location of parts doesn't give patentability over prior art.).

18. As per claim 13:

Abramson and Tran disclosed the method of claim 11, wherein said store data buffer is external to the first storage (Abramson: Figure 3 element 304, column 7 lines 18-26)(The Memory Interface Unit that contains the store data buffer is coupled to the Memory Execution Unit that contains the memory ordering buffer.).

19. As per claim 14:

Abramson and Tran disclosed the method of claim 8 wherein de-allocating the store address from the first storage comprises:

De-allocating the store address from a store address buffer in the first storage (Abramson: Figure 6 element 802; column 8 lines 44-61)(Entries within the store address buffer are inherently de-allocated when the store instruction retires.).

20. As per claim 15:

Abramson and Tran disclosed the method of claim 8 wherein disambiguating the memory renamed load instruction comprises:

Determining whether a store address for the memory renamed load instruction corresponds to a store address in said first storage (Abramson: Figure 11, column 12 lines 32-47 and column 14 lines 19-31)(The speculated load instruction is checked to make sure it obtained the correct data.).

21. As per claim 16:

Abramson and Tran disclosed the method of claim 15 further comprises:

Determining whether said source store address for the memory renamed load instruction is in the second storage (Abramson: Figure 11, column 14 lines 19-44)(The speculated load instruction is checked to make sure it obtained the correct data. If the speculated load gets the incorrect data, then it's determined that the data has already been transferred to the data array, being the second storage.).

22. As per claim 17:

Abramson and Tran disclosed the method of claim 8 further comprising:

Clearing a backend of the processor and restarting the load instruction without memory renaming, if said source store address has been de-allocated from said first storage and said second storage (Abramson: Figure 11, column 14 lines 33-44)(Tran: Figures 2 and 3 element 44, column 11 lines 1-8)(If the data can't be correctly obtained from the first or second data storage, then the instruction would be restarted. Thus, the processor clearing would have occurred with the data sought after being de-allocated from the first and second data storage.).

23. As per claim 18:

Claim 18 essentially recites the same limitations of claim 8. Therefore, claim 18 is rejected for the same reasons as claim 8.

24. As per claim 19:

Claim 19 essentially recites the same limitations of claim 9. Therefore, claim 19 is rejected for the same reasons as claim 9.

25. As per claim 20:

Claim 20 essentially recites the same limitations of claim 10. Therefore, claim 20 is rejected for the same reasons as claim 10.

26. As per claim 21:

Claim 21 essentially recites the same limitations of claim 11. Therefore, claim 21 is rejected for the same reasons as claim 11.

27. As per claim 22:

Claim 22 essentially recites the same limitations of claim 12. Therefore, claim 22 is rejected for the same reasons as claim 12.

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28. As per claim 23:

Claim 23 essentially recites the same limitations of claim 13. Therefore, claim 23 is rejected for the same reasons as claim 13.

29. As per claim 24:

Claim 24 essentially recites the same limitations of claim 14. Therefore, claim 24 is rejected for the same reasons as claim 14.

30. As per claim 25:

Claim 25 essentially recites the same limitations of claim 15. Therefore, claim 25 is rejected for the same reasons as claim 15.

31. As per claim 26:

Claim 26 essentially recites the same limitations of claim 16. Therefore, claim 26 is rejected for the same reasons as claim 16.

32. As per claim 27:

Claim 27 essentially recites the same limitations of claim 17. Therefore, claim 27 is rejected for the same reasons as claim 17.

33. As per claim 28:

Abramson disclosed a computer system comprising:

A processor comprising:

A decoder to decode a load instruction naming a destination register (Abramson: Figure 2 element 201, column 5 lines 12-26)(The load instruction is inherently decoded before it's issued to the execution unit.);

A memory ordering buffer to maintain a store instruction (Abramson: Figure 4

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element 503, column 7 lines 62-67 continued to column 8 lines 1-8); and

A memory coupled to said processor (Abramson: Figure 1 element 214, column 4 lines 35-39).

Abramson failed to teach a trailing store buffer to maintain an address for said store instruction, if said store instruction has been de-allocated from said memory ordering buffer.

However, Tran disclosed a trailing store buffer to maintain an address for said store instruction, if said store instruction has been de-allocated from said memory ordering buffer (Tran: Figures 2 and 3 element 44, column 11 lines 1-8)(The speculative store buffer stores non-speculative stores when a store instruction retires. The store instruction is put into the speculative store buffer at the same time that the data is stored in the data cache. Figure 3 shows the buffer storing the address and the data of the store instruction. It's obvious to one of ordinary skill in the art at the time of the invention that upon the store data being transferred to the data cache, the store instruction has retired, which when in combination with Abramson, results in deallocation of a store entry in the memory ordering buffer.).

The advantage of the speculative store buffer is that it stores the most recent data values for memory addresses, thus only a single hit for a memory address is allowed, which reduces complexity and allows for increased performance (Tran: Column 3 lines 16-35). One of ordinary skill in the art would have been motivated to add the speculative store buffer for the advantage of increased performance. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to

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implement a speculative store buffer for the advantage of increased performance for memory operations.

34. As per claim 29:

Claim 29 essentially recites the same limitations of claim 2. Therefore, claim 29 is rejected for the same reasons as claim 2.

35. As per claim 30:

Claim 30 essentially recites the same limitations of claim 3. Therefore, claim 30 is rejected for the same reasons as claim 3.

Response to Arguments

36. The arguments presented by Applicant in the response, received on 2/16/2007 are not considered persuasive:

37. Applicant argues "Tran failed to teach a trailing store buffer to maintain an address for said source store instruction, if said source store instruction has been deallocated from said memory ordering buffer."

This argument is not found to be persuasive for the following reason. The load/store buffer of Tran acts in similar ways that the memory-ordering buffer of Abramson does in that it deallocated a store entry when the instruction is retired and the data is saved to the data cache. Tran disclosed that when the store instruction is retired from the load/store buffer, it's also stored within the speculative store buffer at the same time (Tran: Column 11 lines 1-8). Applicant attempts to refute that this is the case by citing another embodiment of Tran that doesn't store the data in the speculative store

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buffer at the same time. However, this is just an alternative embodiment and not the embodiment that was originally cited by the examiner. Thus, Tran correctly reads upon the claimed limitation.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

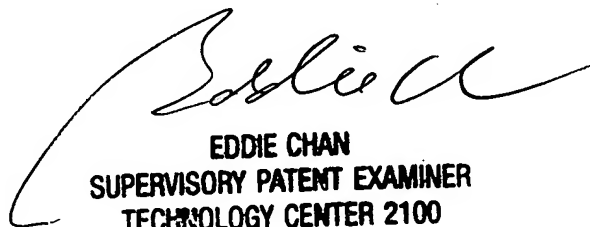
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183



EDDIE CHAN
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